Application of the Copper Damascene Process for the Preparation of Electromigration Test Structures

M. Stangl, J. Acker, V. Hoffmann, K. Wetzig, U. Künzelmann, J.W. Barth

a IFW Dresden, P.O. Box 270116, D-01171 Dresden, Germany
b University of Applied Sciences Lausitz, P.O. Box 101548, D-01958 Senftenberg, Germany
c Dresden University of Technology, IHM, D-01062 Dresden, Germany

E-mail: m.stangl@ifw-dresden.de

The damascene technology is widely used for Cu interconnect structures in integrated circuits. Due to the strong variation of the feature sizes and densities of Cu interconnect lines and contact pads involved in electromigration (EM) test structures, the CMP of the excessive Cu layer is very complicated. This paper will present the challenges of removing of Cu and Ta by CMP and the successful application of well prepared Cu interconnects in life-time experiments.

Keywords: Copper, Damascene process, CMP, Edge erosion, Surface finish, Electromigration

1. Introduction

Copper represents the favoured conducting material for interconnect metallisations in modern ultra large scaled integrated (ULSI) semiconductor devices [1]. For the preparation of buried Cu structures in damascene technology, the CMP process represents a determining factor regarding a good life-time performance of high loaded interconnect lines [2]. Due to the complex layout of NIST (National Institute of Standards and Technology) test structures according Fig. 1 some CMP specific difficulties had to be considered. This paper will discuss the challenges for residuelessly preparation of the test structures, for dishing, edge erosion, and a good finish quality. Reasonable solutions have been found by interactively optimising the CMP process parameters, i.e. load, backside pressure, rotation speed of platen and carrier as well as the definition of the switching point between both, the copper and the barrier slurries. Finally, the successful application of interconnect lines will be presented in form of EM life-time experiments.

Fig. 1 SEM top view image after CMP of a Cu damascene NIST test structure.
The contact pads are used for power input and measuring of resistivity during life-time experiments.
2. Preparation of Cu damascene interconnect structures

The preparation of Cu interconnects in damascene technology was performed using 4 inches Si (100) wafer substrates with a 1 µm SiO₂ layer as dielectric. Reactive ion etching was applied for creation of trenches with a minimum feature size of 0.4 µm and a depth up to 0.8 µm. Subsequently, a 50 nm Ta diffusion barrier and a 100 nm Cu seed-layer were deposited by magnetron sputtering (MS) without vacuum break. The trench filling with Cu was performed in two different ways: electrochemical deposition (ECD) and physical vapour deposition (PVD). CMP was applied for the removal of excessive Cu. Scanning electron microscopy (SEM) (Zeiss Gemini 1530 and FEI XL 40) and focused ion beam (FIB) technology (Zeiss CrossBeam 1540 XB) were used for characterisation of Cu interconnects in top view and cross section. The final passivation of the wafer surface in form of a SiNₓ/SiO₂/SiNₓ 3 layers stack was carried out by chemical vapour deposition (CVD). The schematic build-up and a real cross section image of a Cu damascene structure are shown in Fig. 2.

![Schematic build-up and real SEM cross section image of a Cu damascene interconnect with SiNₓ/SiO₂/SiNₓ caplayer.](image)

3. Challenges for the CMP process

The polisher MEGAPOL E460 (Fa. PRESI) with platen diameter of 60 cm and a 4 inches carrier was applied for the CMP process. Generally, the CMP was performed in two sections in several time steps:

i) copper polish in several steps followed by

ii) Ta-barrier polish at the same platen

with the respective slurry from i-Cue® system from Cabot Microelectronics Corporation. The pad (type IC 1000 with sub-pad Suba IV and c-grooves, Rodel Nitta) was conditioned prior to each CMP process with a crossed diamond knife tool under a strong deionised (DI) water jet. This procedure was repeated periodically in the case of long-time polish action as well as before the slurry was changed from copper to the barrier slurry. Each single polishing step was succeeded by a 30 s buffing step with 0.25 bar pressure and the addition of pure DI water.
The first and the majority of the copper polishing experiments were carried out using the slurry i-Cue® 5003 with the addition of a 30% hydrogen peroxide H₂O₂ solution in the v/v-mixing ratio 11.9 : 1 (slurry : oxidising solution) and for some additional experiments with the slurry i-Cue® EP-C7092 mixed with 30% H₂O₂ in the ratio of 31.3:1. A flow rate of 150 ml/min was used. In order to create a reproducible initial state, the pad was conditioned by polishing an unstructured copper dummy wafer just before polishing the process wafer.

The polishing action of the slurry is a complex process of copper oxidation, its chemical and mechanical removal as well as the stabilisation of the removed products. The removal rate \( v_r \) is mainly determined by the rotation speeds of the platen \( \omega_p \) and the carrier \( \omega_c \) as well as by the polishing pressure (or load) \( p_a \). The application of an additional back side pressure \( p_b \) through concentrically arranged thin holes in the carriers bottom influences the curvature. It can be used to correct the \( v_r \)-distribution within the wafer diameter.

In order to estimate \( v_r \) and its distribution in dependence of the set of polishing parameters for the two differently applied Cu-layers, experiments with unstructured wafers have been carried out preliminarily. The thickness of the Cu-layer was measured electrically by a four point resistivity mapping system (CDE ResMap 178). With \( p_a = 0.5 \) bar and \( \omega_p = \omega_c = 40 \) rpm removal rates of roughly 150 nm/min and 200 nm/min had been measured for ECD-Cu- and PVD/MS-Cu-layers, respectively. The higher value for \( v_r \) in the case of the PVD/MS-Cu might be due to the higher quantity of the grain boundaries at the metal surface in contrast to the ECD-Cu with larger grains.

The ECD or PVD Cu film of roughly 2 µm thickness had to be polished down to final thicknesses between 400 – 800 nm. Therefore, some initial experiments were necessary to optimise the parameter sets for the pressures within the ranges of \( (0.7 > p_a > 0.5) \) bar and \( (0.07 > p_b > 0.02) \) bar at \( \omega_p = \omega_c = 40 \) rpm. The Cu-polish was performed in time cycles of a few minutes down to two minutes with intermediate visual control of the results and correction of \( p_a \). Even with a relatively high selectivity of the removal rates between Cu and Ta for the Cu-slurry used, it was difficult to correct the wafer bow exactly and to avoid Cu over-polish. Due to high differences of the structure densities at the wafer layout, there were some local differences of the removal, too.

The barrier-slurry i-Cue® 5220 (polishing parameters: slurry flow 150 ml/min; \( (0.6 > p_a > 0.5) \) bar and \( (0.06 > p_b > 0.05) \) bar, \( \omega_p = \omega_c = 40 \) rpm) contains no additional oxidising agent, proceeds mainly mechanically and so its selectivity to Cu is low. In order to avoid over-polish in the copper polish, in some cases we tried to remove very thin Cu residuals even in this barrier removal step. It succeeded in some cases, only.

Therefore the very last Cu-polishing step was performed with a different Cu-slurry (development product i-Cue® EP-C7092) which targets to improved planarity for the 65 nm technology node. In contrast to the commercial i-Cue® 5003 slurry, the removal rate for areas of high and low structure density was better balanced and as a consequence there were lower in-homogeneities of the Cu removal at the surface of the wafers.
As shown in Fig. 1, the principal layout of the EM NIST structures involves large differences of the structure density, e.g. large pads next to narrow EM lines. Hence, during the preparation some aspects of the local homogeneity had to be considered:

i) Complete removal of copper and barrier layer residuals from the EM lines in order to avoid shortcuts.

ii) Prevention of the dishing at contact pads in order to provide good bondability.

iii) Minimising of erosion at edges and local areas in order to increase the reliability and precision of the EM measurements.

Mostly, Cu-residuals on the EM lines could be avoided. In some cases dishing of the contact pads appeared. It was possible to minimise by reducing the polishing time and pressure with interactive inspection of the polishing results. According to Fig. 3 (FIB cross section of an EM line), CMP induced defects near the transition area Cu/Ta/SiO₂ as well as preferred etching of grain boundaries had been found partially.

Fig. 3 CMP induced defects at the transition area Cu/Ta/SiO₂ and indicated preferred etching of grain boundaries.

Furthermore, some preparations showed scratches at the surface of copper lines and pads after the barrier removal (Fig. 4a). Possibly they are induced by residuals accumulated in eroded areas during the copper polishing procedure. Scratch free Cu surfaces (Fig. 4b) could be obtained by stepwise reduction of the polishing pressure during the very end of the Cu polish. In addition, the use of the slurry i-Cue® EP-C70921 in this phase provided good results.

Fig. 4a SEM image of the wafer surface after CMP with scratch formations.  Fig. 4b SEM image of the wafer surface after CMP with excellent finish quality.

After all CMP processes the surfaces was scrubbed thoroughly with a PVA brush (Rippey, Microclean) and manually wiped with a soft clean room tissue under DI water. Finally the wafers were ultrasonically cleaned in DI water and dried at room temperature in a spin processor.
4. Conclusion

After a series of initial experiments with partially occurring overpolish, the dishing of the contact pads could be minimised even in the case of complete CMP of the narrowest interconnect lines with 0.4 µm feature size. Erosion and scratch formation had been practically avoided. The final test structures had been found to be well suited for the respective EM experiments. Referring to this, Fig. 5 illustrates electrical resistivity measurements showing a better life-time performance for capped interconnect lines due to suppressed surface diffusion processes [3,4]. From the mean time to failure (MTTF) of an ensemble of lines as a function of temperature 1000/T, the activation energy Q can be calculated from the slope according to Black’s law (Eq. 1) [5-7]. Here, A represents a geometry dependent constant, j the current density, and k the Boltzmann constant.

\[
\text{MTTF} = A j^{-n} \left( \frac{Q}{kT} \right)
\]  

The investigations were focused on Cu lines with low (A) and high (B) content of chlorine, sulphur, and carbon impurities incorporated during electrochemical deposition [8,9]. Cu interconnects containing more impurities exhibited lower activation energies for the EM damage (Fig. 6). Consequently, pure Cu metallisation structures sustain 200 K higher temperatures during the application of a current density of 6 MA/cm².

The damage of Cu interconnects during life-time experiments is induced by a material transport and void formation. Preferably, these voids are developed at the Cu/SiNₓ interface due to thermally induced stresses because of large differences of the thermal coefficient of expansion (TCE) for Cu and SiNₓ [7]. FIB investigations revealed this process as shown in Fig. 7. Possibly, the weakening of the Cu/SiNₓ interface results also from remaining impurities after the CMP process. Therefore, an adequate surface cleaning procedure before deposition of passivating films is of great importance for a good EM performance of Cu interconnects.
Fig. 7 FIB cross section image through a damaged Cu interconnect after an EM experiment; left: starting formation of voids, right: total damage of the Cu line.

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