This paper presents the first successful attempt to integrate crystalline high-K gate dielectrics into a virtually damage-free damascene metal gate process by means of front-end chemical mechanical planarization. Process details as well as initial electrical characterization results on fully functional gate Gd$_2$O$_3$ dielectric MOSFETs with equivalent oxide thickness (EOT) down to 1nm are discussed.

Keywords: chemical mechanical planarization, CMP, high-k gate dielectrics, metal gate MOSFET, damascene metal gate technology

1. Introduction

Ever increasing gate leakages through ultra-scaled SiO$_2$ gate dielectrics have led to extensive investigation of alternative materials with higher dielectric permittivity (high-K) in order to extend the unprecedented growth of IC complexity of the last four decades into the future.

Recently, very promising properties of epitaxially grown, crystalline rare-earth metal-oxides have been reported [1] and the integration of Pr$_2$O$_3$ dielectric in a conventional polysilicon CMOS process was successfully demonstrated [2]. However, high temperature annealing [3] and aggressive reactive ion etching (RIE) was found to degrade the initial quality of the sensitive high-K gate stack [2]. In order to minimize process induced oxide damage (PIOD), we have integrated crystalline high-K dielectrics into a virtually damage-free replacement gate process [4, 5]. For the first time, fully functional metal gate MOSFETs with crystalline Gd$_2$O$_3$ dielectric have been fabricated by means of front-end chemical mechanical planarization (CMP) in a “gentle” damascene metal gate technology.

2. Device Fabrication

The basic process concept of the damascene metal gate technology is shown in Fig. 1. Processing is performed on 4 inch p-type Si (100) wafers. Initially, dummy gate stacks are formed by consecutive deposition of silicon nitride and polysilicon, lithography and reactive ion etching (RIE) (Fig. 2a), followed by self-aligned S/D ion implantation. Next, the CVD alignment-oxide is deposited and RTA anneals at 1000°C are performed to activate S/D implants.
Figure 1. Basic concept of the damascene metal gate process: A so-called ‘‘dummy gate’’ acts as a placeholder for the final gate stack (1) After having performed all aggressive process steps as RIE and high temperature anneals, the dummy gate can be removed by leaving a self-aligned imprint of the gate stack in the oxide. (2) Subsequently, the high-K gate dielectric and metal gate are deposited. (3) The initial material quality of the crystalline high-K gate dielectric is largely preserved damascene metal gate processing.

The oxide is planarized by CMP down to the gate level using a atomic force microscope-based ex-situ endpoint detection. The dummy gates are removed completely by wet chemical etching, leaving a self-aligned imprint of the gate stack on the oxide layer (Fig.2b).

Figure 2. Atomic force microscopy (AFM) image of a dummy gate structure (a) and a self-aligned imprint of the gate stack in the alignment oxide (b).

Subsequently, crystalline Gd$_2$O$_3$ layers of 5.3 nm and 13.5 nm physical thickness are grown by molecular beam epitaxy (MBE) with smooth surface topography and good leakage currents as evident from AFM and Conductive-AFM measurements (Fig. 3). In addition, wafers with conventional SiO$_2$ are fabricated as a reference. Tungsten is deposited on top of the gate dielectrics and CMP is used to pattern the damascene metal gates. Standard back-end processing completes the fabrication.
3. Results and Discussion

The fabricated devices with Gd₂O₃ gate dielectric and tungsten gate electrode are fully functional. CV measurements on Gd₂O₃ capacitors give a dielectric constant of 10.4, corresponding to EOTs of 1.9 nm and 5.1 nm respectively. Leakages are below $1 \times 10^{-1}$ A/cm² for the 1.9 nm Gd₂O₃ and $1 \times 10^{-3}$ A/cm² for the 5.1 nm, respectively, (Fig. 4), consistent with leakage requirements set by the ITRS [6]).

Figure 5. Gate leakage currents of 1.9 nm and 5.1 nm metal gate Gd₂O₃ pMOS capacitors (gate injection, substrate in accumulation).

The Gd₂O₃ gate dielectric nMOSFETs show proper transistor behavior (Fig. 6 and 7).

Figure 6. Output characteristics of a metal gate Gd₂O₃ nMOSFET.
Note that extremely low hysteresis of less than 30 mV is observed in the subVt characteristics (Fig. 7), which is a substantial improvement when compared to conventionally integrated high-K oxides [7]. In the case of process-damaged high-K oxides, large hysteresis effects with Vt-shifts of more than 300 mV have been observed which could be related to a large susceptibility to build-up charge trapping sites [7]. The subVt swing of approximately 130 mV/dec indicates high interface state densities. Charge pumping (CP) measurements revealed trap densities of $2.3 \times 10^{12} \text{ eV}^{-1} \text{cm}^{-2}$, consistent with the degraded subVt swing. However, only slightly reduced values of $1.8 \times 10^{12} \text{ eV}^{-1} \text{cm}^{-2}$ are obtained for the SiO$_2$ reference devices which puts in question the effectiveness of the forming gas anneal when using tungsten gates. Energy resolved CP measurements on Gd$_2$O$_3$ nMOS devices showed that most of the interface traps are located in the upper half of the band gap (Fig. 8).

Effective mobilities of 130 cm$^2$/Vs have been measured for the Gd$_2$O$_3$ MOSFETs as shown in Fig. 9.
Figure 9. Measured effective electron mobilities of damascene metal gate Gd$_2$O$_3$ nMOSFETs (EOT=5.1 nm).

Compared to SiO$_2$ references this corresponds to a reduction of approx. 40% at the same effective electric field. We suspect that the acceptor-type interface states significantly degrade mobility due to Coulomb-scattering.

4. Conclusion

We have successfully integrated crystalline Gd$_2$O$_3$ with EOT of 1.9 nm in a damascene metal gate process by means of chemical mechanical planarization. Since the harsh processing is done prior to high-K deposition, PIOD-effects are minimized and the initial material quality of the crystalline high-K gate dielectric is largely preserved, so that the progress in high-K material engineering can be monitored directly at the device level.

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References