Preface

"CMP, the Technology of Pleasant Surprise and Promise of the Future"

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It was 20 years ago when a couple of visitors came to my office at Hewlett-Packard with a unique proposal in which they wanted to planarize the top surface of integrated circuits to replace existing technology such as glass reflow and dummy oxide for global planarization in order to make the surface almost optically flat. That was the proposal which we call CMP today.
In 1981 at the first ramp session of IEDM, we discussed about futures of a variety of technology and device structures for sub micron geometry integrated circuits. Among the questions raised and discussed, one of the hot topics was how far optical lithography can go. It was still before the excimer laser based lithography came up to the horizon, and commonly accepted limit for i-line lithography was about one micron for practical surface of integrated circuits. As one of the ramp session panel members, I did some preparation by asking optical lens designers in Japan about what could possibly make optical lithography go into submicron range. He said, "If you can make the surface of integrated circuits wafer optically flat, optical lithography can do 0.1um geometry. It was at least for me a striking statement.
As we all know today, CMP is the technology which make this real, i.e. by making the surface of integrated circuits almost optically flat and helped optical lithography extend its life way beyond sub-tenth micron barrier.

However, in the beginning of CMP era, many experts in semiconductor processing were very skeptical about the future of CMP when it was introduced. Major reason was somewhat psychological, i.e. the most sensitive surface of semiconductor devices may not withstand against chemico-mechanical polishing which was believed to be only applicable for wafer thinning from the back surface. CMP inventors and engineers who brought the technology as we see today went through difficult time in early 90's.

As we look ahead the forthcoming era of nanoscale science and engineering, CMP technology will further contribute in a variety of ways. Three dimensional device structures to extend the scaled CMOS, such as the FinFET, the trigate MOSFET, and SOI definitely need CMP, and also revolutionary nanodevices by using nanowires and nanotubes would extract their advantage when they are used as vertical charge controlled devices by using CMP capability. Newly emerging opportunities in the area of bio-, medical-MEMS devices would make nanofluidic structures by the combination of silicon etching and CMP. Possible implementation of photonic crystal based devices, once needs arise toward integration with electronics, would most likely demand CMP capability. Most of three-dimensional integration of integrated circuits does rely upon CMP to stack a layer on top of the layer.

Being said the above, there will be a significant challenge for CMP technology community, which is a large variety of materials to be polished, and therefore a number of combinations of slurry materials and their treatment to fulfill technical and environmental needs before those processes come to manufacturing floor.

It will be a tough period in front of us with increasingly strong demand for control of polished surfaces, defects, and cost, but I believe the CMP community who has always made break through from the very beginning until today will meet the challenge and keep the pace of finding solutions for the future.