■「CMP Process Modeling for Improved Process Integration, Development and Control」

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Chemical mechanical planarization continues to be one of the more challenging processes in semiconductor manufacturing. It is still considered the leading planarization technology for current and future manufacturing. The continuous drive to reduce critical dimensions, introduce new materials and process consumables, and increase productivity create constant pressure on the research community to develop new tools and techniques for improving CMP. At the basis of this improvement must be improved understanding of the CMP process. In order to guarantee that CMP can keep up with the challenges, the use of comprehensive and integrated process models are of great interest.

Industry feedback, through discussion and ITRS Roadmap materials, highlights their expectations for modeling of this critical process. There is a general view that, as it now stands, models are not reliable enough to be used as verification of the process. The usefulness of modeling is seen as the ability to give feedback for "what-if" scenarios (for example, predicting "polishability" of new mask designs) in lieu of time-consuming DOE tests. Models should give some performance prediction for realistic, heterogeneous pattern effects. Models should predict not only wafer scale phenomena but also have some capability to capture feature/chip scale interaction.

Recent discussions to develop a "roadmap" for CMP modeling have laid out some of the expectations and requirements for useful CMP models. The overriding requirements can be summarized by the following: first, models must be able to address multi-scale (wafer-, die-, feature-level) and, second, these model capabilities must be integrated for global CMP modeling to be useful including linkage of CMP models to upstream (deposition, etc.) and downstream (lithography, etc.) processes. Application areas of interest for models include process control, feedback for design, control and process optimization, and tool and consumable design. The emphasis of such models should be focused over a wide range of topics and should be multi-scale (or integrated). The modeling is needed specifically for Cu pattern effects (not necessarily just density) as based on "heterogeneous" patterns, loading effects and responding to decreasing wire thicknesses. Models should be linked to upstream processes (HDP, Cu-deposition) as well as downstream processes (lithography) in order to allow series process improvement with the interaction effects considered. Remaining as a key concern is understanding of the fundamental mechanisms of MRR in CMP (specially the effects of the chemistry) and in particular in the presence of a host of new materials (low k dielectrics for example) and pad geometries and materials (consider response beyond simply elasticity and temperature invariant), and slurry delivery as by porous media flow and micro-fluidics. Finally, defectivity models for which performance vs. defectivity can be assessed to link design to device performance is of interest.

There are issues at three scales of CMP to be modeled, namely, the particle scale, feature & die scale and wafer scale. Models at the particle scales are needed to address the roles and interactions of slurry particles, slurry chemicals, polishing pad and wafer materials. Models at the feature and die scales are needed to address the topography evolution of integrated circuit (IC) chips as a function of pattern density, line width, pitch width and polishing time. The final goal of modeling efforts at this scale is to facilitate the development of electronics design automation (EDA) or electronics computer aided design (ECAD) software tools in terms of design for manufacturability. Wafer-scale models address the issues related to the material removal non-uniformity over the wafer surface.

The past research work reported in the literature over the last decade or so has established a number of basic modeling approaches with differing capabilities for simulation of aspects of CMP. Many of these start with Preston's equation-based approaches. The more innovative work has also proposed strategies for designing process consumables (particle size and distribution or pad surface topography, for example) for optimal performance. The next efforts will be directed towards continued expansion of the CMP model and integration of CMP process modeling with process (machinery and recipes) and device design and optimization stages.

This CMP committee of JSPE is expected to contribute in a substantial way to the development and validation of these models with the end result being to further the understanding of CMP and to advance CMP technology.